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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
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EXAMINER	
ZAMAN, FAISAL M	

ART UNIT	PAPER NUMBER
2112	

DATE MAILED: 02/28/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/811,410	KATAOKA, TOSHIHIKO	
	Examiner	Art Unit	
	Faisal Zaman	2112	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *03 January 2006*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-17* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-4 and 10-18* is/are rejected.

7)☒ Claim(s) *5-9* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *26 March 2004* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☒ Other: See Continuation Sheet

DETAILED ACTION

Response to Arguments

1. Applicant's arguments, see pages 24-28, filed 1/03/2006, with respect to Claims 5-9 have been fully considered and are persuasive. The rejection of 9/27/2005 has been withdrawn.

2. Applicant's arguments filed 1/03/2006 have been fully considered but they are not persuasive.

As currently amended, Claims 1 and 11-14; and Claims 2-4, 10, and 18 are substantially similar to each other but where the terms "data" and "resource" are used in place of each other. Claims 15-17 are substantially similar, but where the terms "data" and "resource" are used together. Applicant's argument that the act of acquiring resource(s) and the act of acquiring data are distinguishable is not persuasive in the context of the claims. As is well known in the art in the types of systems disclosed in the references used in the rejections, acquiring a resource can be analogous to acquiring data. This can be shown in the Microsoft Press Computer Dictionary, Second Edition, 1994, on page 339 under the definition of "resource" and further under the definition of "resource data". In addition, in the context of the Applicant's specification (see page 10, lines 7-13), acquiring a resource includes acquiring data. Therefore, on the basis that the references used in the rejections of the claims teach acquiring data but not acquiring a resource, the claims stand rejected.

Regarding Claims 2-4, and 10, Applicant's argument that Reid indicates that the interrupt triggering event is not a packet of data being received, but rather the completion of a DMA cycle, with the interrupt that is delayed being a DMA completion interrupt that is delayed to allow for the accumulation of additional data packets (see page 22 of Applicant's arguments filed 1/03/2006), the interrupt being generated after the completion of a DMA cycle is merely a different embodiment of the disclosure of Reid. As shown in Column 4, lines 18-21, the embodiment that the examiner uses in the rejection of Claim 2 in the Office Action dated 9/27/2005, is where an interrupt is generated after a certain time elapses from when data is generated. Regarding Applicant's argument that the interrupt delay time of Reid is determined in response to the accumulation of a number of data packets, so that it cannot be predetermined (see page 22 of Applicant's arguments), Reid discloses that the number of packets requiring interrupts is known and the interrupt is generated once that known number of packets is accumulated (ie. a predetermined delay time) (see Column 9, lines 10-15).

Therefore, because of the above reasons, Claims 1-4 and 10-18 stand rejected under 35 USC 103(a).

3. As currently amended, the objections to the specification and rejections to Claims 1- 17 under 35 USC 112, second paragraph, are withdrawn.

Claim Objections

4. Claim 10 recites the limitation "said resource" in lines 4, 5, 7, and 8. There is insufficient antecedent basis for this limitation in the claim.

Claim Rejections - 35 USC § 103

5. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 1, 2-4, 10, and 12-17 are rejected under 35 USC 103(a) as being obvious over Hashimoto et al. ("Hashimoto") (U.S. 6,397,282) in view of Williams et al. ("Williams") (U.S. 6,167,480), and further in view of Reid et al. ("Reid") (U.S. 6,115,776).

Hashimoto discloses the invention substantially as claimed.

Regarding Claims 1 and 12, Hashimoto discloses:

An interrupt control device (Fig. 3, item 20, Column 2, lines 23-29) for issuing interrupts to a central processing unit, comprising:

An object acquiring unit (Fig. 3, item 22, Column 11, line 1) for acquiring resource(s) for use by said central processing unit;

An interrupt issuing unit for issuing an interrupt to said central processing unit before said object acquiring unit acquires said resource, said interrupt indicating that said resource has become available (Fig. 3, item 26, Column 11, lines 15-19);

Hashimoto does not disclose expressly:

A use delay unit for delaying the use of said resource by said central processing unit until said object acquiring unit acquires said resource if said central processing unit which has received said interrupt requests the use of said resource before said object acquiring unit acquires said resource; and

Wherein said interrupt issuing unit issues said interrupt after a predetermined setup period elapses from when a data generation device generating said data starts to generate said data.

In the same field of endeavor (e.g. providing an interrupt signal to a host system processor), Williams discloses a use delay unit (Column 3, lines 8-21) for delaying the use of said resource by said central processing unit until said object acquiring unit acquires said resource if said central processing unit which has received said interrupt requests the use of said resource before said object acquiring unit acquires said resource.

Also in the same field of endeavor (e.g. improvements to the transmission of information between digital devices over a communications medium), Reid discloses wherein said interrupt issuing unit (Reid, Column 9, lines 6-15) issues said interrupt after a predetermined setup period elapses from when a data generation device generating said data starts to generate said data.

Accordingly, it would have been obvious to one of ordinary skill in the art at the time of the invention was made to have incorporated Williams' teachings of providing an interrupt signal to a host system processor with the teachings of Hashimoto, for the

purpose of providing only a single interrupt for an incoming information packet's reception (see Williams, Column 4, lines 8-10) and Reid's teachings of improvements to the transmission of information between digital devices over a communications medium with the teachings of Hashimoto, for the purpose of reducing "the number of interrupts generated by the network to the processor and to thereby reduce the processing burden to the operating system of servicing those interrupts" (Reid, Column 3, lines 29-31). Also, it would have been desirable as stated by Williams for a network peripheral to be able to provide such an interrupt for information packets that conform to a user specified network operating system protocol (see Williams, Column 4, lines 8-26). Hashimoto provides motivation to combine by making a point of his invention to be able to postpone interrupt requests that do not require immediate attention (see Hashimoto, Column 2, lines 10-22).

Regarding Claim 2, Hashimoto discloses:

An interrupt control device (Fig. 3, item 20, Column 2, lines 23-29) for issuing interrupts to a central processing unit, comprising:

An object acquiring unit (Fig. 3, item 22, Column 11, line 1) for acquiring data for use by said central processing unit;

An interrupt issuing unit for issuing an interrupt to said central processing unit before said object acquiring unit acquires said data (Fig. 3, item 26, Column 11, lines 15-19);

Hashimoto does not disclose expressly:

A use delay unit for delaying the use of said data by said central processing unit until said object acquiring unit acquires said data if said central processing unit which has received said interrupt requests the use of said data before said object acquiring unit acquires said data; and

Wherein said interrupt issuing unit issues said interrupt after a predetermined setup period elapses from when a data generation device generating said data starts to generate said data.

In the same field of endeavor (e.g. providing an interrupt signal to a host system processor), Williams discloses a use delay unit (Column 3, lines 8-21) for delaying the use of said resource by said central processing unit until said object acquiring unit acquires said resource if said central processing unit which has received said interrupt requests the use of said resource before said object acquiring unit acquires said resource.

Also in the same field of endeavor (e.g. improvements to the transmission of information between digital devices over a communications medium), Reid discloses wherein said interrupt issuing unit (Reid, Column 9, lines 6-15) issues said interrupt after a predetermined setup period elapses from when a data generation device generating said data starts to generate said data.

Accordingly, it would have been obvious to one of ordinary skill in the art at the time of the invention was made to have incorporated Williams' teachings of providing an interrupt signal to a host system processor with the teachings of Hashimoto, for the purpose of providing only a single interrupt for an incoming information packet's

reception (see Williams, Column 4, lines 8-10) and Reid's teachings of improvements to the transmission of information between digital devices over a communications medium with the teachings of Hashimoto, for the purpose of reducing "the number of interrupts generated by the network to the processor and to thereby reduce the processing burden to the operating system of servicing those interrupts" (Reid, Column 3, lines 29-31). Also, it would have been desirable as stated by Williams for a network peripheral to be able to provide such an interrupt for information packets that conform to a user specified network operating system protocol (see Williams, Column 4, lines 8-26). Hashimoto provides motivation to combine by making a point of his invention to be able to postpone interrupt requests that do not require immediate attention (see Hashimoto, Column 2, lines 10-22).

Regarding Claim 3, Reid disclose the following limitations, which are not disclosed expressly in Hashimoto and Williams:

A time difference measuring unit (Reid, Column 9, lines 6-15) for measuring a time difference between when said object acquiring unit acquires said data and when said central processing unit which has received said interrupt requests the use of said data; and

A setup period change unit (Reid, Column 9, lines 27-29) for changing said predetermined setup period according to said time difference.

The motivation that was utilized in the combination of Claim 1, super, applies equally as well to Claim 3.

Regarding Claim 4, Williams discloses an acquisition time measuring unit (Figure 11, item 270, Column 14, lines 14-18) for measuring an acquisition time from when said data generation device starts to generate said data until said object acquiring device acquires said data;

Wherein said setup period change unit changes said setup period according to said acquisition time and said time difference.

Please note the definition of "latency" as used in the reference in this rejection can be found at <Hyperdictionary.com>. The portion of the claim regarding the setup period change unit is rejected because it would be obvious to one of ordinary skill in the art that said acquisition time and the said time difference are directly related, therefore the supporting rationale of the rejection to Claim 3 applies equally as well here.

The motivation that was utilized in the combination of Claim 1, super, applies equally as well to Claim 4.

Regarding Claim 10, Hashimoto does not disclose a setup period change unit for, (i) changing said setup period to a smaller value if said central processing unit which has received said interrupt requests the use of said data or said resource before said object acquiring unit acquires said data or said resource, and (ii) changing said setup period to a greater value if said central processing unit which has received said interrupt requests the use of said data or said resource after said object acquiring unit acquires said data or said resource.

However, in the same field of endeavor, Reid discloses a setup period change unit which has a delay that may be user-programmable, or it may be system-programmable based on varying system parameters (Reid, Column 6, lines 36-37). Reid further discloses a setup period change unit that is able to generate an interrupt after a said number of packets accumulates or after a predetermined period of time elapses (Reid, Column 9, lines 13-15).

Accordingly, it would have been obvious to one of ordinary skill in the art at the time of the invention was made to have incorporated Reid's teachings of delaying interrupts until a predetermined number of data packets accumulates or a predetermined period of time elapses to the teachings of Hashimoto for the purpose of increasing or decreasing the number of data packets that are stored in storage (Hashimoto, Column 11, line 1) before an interrupt is sent to the central processing unit.

The motivation that was utilized in the combination of Claim 1, super, applies equally as well to Claim 10.

Regarding Claims 13 and 14, all the same elements of Claims 3 and 4, respectively are listed, but where "data generation device" is replaced with "resource reservation device". Since "data" and "resource" were used interchangeably in the specification and based on examiner's response above, the supporting rationale of the rejection to Claims 3 and 4 apply equally as well to Claims 13 and 14, respectively.

Regarding Claim 15 all the same elements of Claim 1 are listed, but where the central processing unit and interrupt control device are located in an information processing device. Since it would be obvious to one of ordinary skill in the art that a central processing unit and interrupt control device would be located in some sort of an information processing device, the supporting rationale of the rejection to Claim 1 applies equally as well to Claim 15.

Regarding Claim 16 all the same elements of Claim 1 are listed, but in method form rather than system form. Therefore, the supporting rationale of the rejection to Claim 1 applies equally as well to Claim 16.

Regarding Claim 17 all the same elements of Claim 1 are listed, but in program product form rather than system form. Therefore, the supporting rationale of the rejection to Claim 1 applies equally as well to Claim 17.

Claim Rejections - 35 USC § 103

6. **Claims 11 and 18** are rejected under 35 USC 103(a) as being obvious over Hashimoto-Williams in view of Reid and in further view of Brice, Jr. et al. ("Brice") (U.S. 6,754,738).

Hashimoto-Williams discloses the invention substantially as claimed.

Hashimoto-Williams discloses a delay processing unit for (ii) causing said central processing unit to return from interrupt handling caused by said interrupt, to delay the use of said data or said resource by said central processing unit until said object acquiring unit acquires said data or said resource (Hashimoto, Figure 5, Column 8, lines 1-24). However, Hashimoto-Williams do not disclose expressly a delay time calculation unit for calculating a delay time required from the time said object acquiring unit receives a request for use of said data or resource from said central processing unit which has received said interrupt until said object acquiring unit acquires said data or resource as well as a delay processing unit for (i) causing said central processing unit to use polling to request said data or said resource if said delay time is less than a predetermined threshold.

In the same field of endeavor (e.g. improvements to the transmission of information between digital devices over a communications medium), Reid discloses a delay time calculation unit (Column 10, lines 8-18) for calculating a delay time required from the time said object acquiring unit receives a request for use of said data or resource from said central processing unit which has received said interrupt until said object acquiring unit acquires said data or resource.

Accordingly, it would have been obvious to one of ordinary skill in the computer architecture art at the time the invention was made to have incorporated Reid's teachings of a computer operating system in which interrupts are generated to a processor by events which then require processor time to service to the teachings of Hashimoto and Williams, for the purpose of delaying data to be sent to the processor

until a predetermined amount of data segments or a predetermined time has elapsed (Reid, abstract, Brice, abstract). Hashimoto-Williams provides motivation to combine by stating that interruption requests that do not require immediate attention are postponed from being sent to the central processing unit a predetermined delay has elapsed (Hashimoto, Column 2, lines 10-22).

In the same field of endeavor, Brice discloses a delay processing unit (Brice, Column 11, lines 28-32) for (i) causing said central processing unit to use polling to request said data or said resource if said delay time is less than a predetermined threshold.

The motivation that was utilized in the combination of the previous part of the claim, super, applies equally as well to this part of the claim.

Regarding Claim 18 all the same elements of Claim 11 are listed, but where "resource" is replaced with "data". Since "resource" and "data" were used interchangeably in the specification and based on examiner's response above, the supporting rationale of the rejection to Claim 11 applies equally as well to Claim 18.

Allowable Subject Matter

7. **Claims 5-9** are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

The following is a statement of reasons for the indication of allowable subject matter: the prior art of record does not teach the following limitations:

An interrupt issuing unit issues an interrupt to a central processing unit before an object acquiring unit acquires each of a plurality of data segments, each said interrupt indicating that the respective one of said plurality of data segments has become available;

A time difference measuring unit measures, for each of said plurality of data segments, the time difference between when said object acquiring unit acquires said data segment and when said central processing unit which has received said interrupt requests the use of said data segment; and

A setup period change unit changes a setup period according to the time differences measured by said time difference measuring unit.

Conclusion

8. "Computer Dictionary", Second Edition, by Microsoft Press, 1994, page 339 is cited as Relevant Art.

9. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. Jinzaki (U.S. Publication No. 2004/0236875) discloses a computer for determining interruption delay dynamically. Williams et al. (U.S. 5,881,296) discloses a method for improved interrupt processing in a computer system. Huffman et al. (U.S. 6,640,274) discloses a method and apparatus for reducing the disk drive data transfer interrupt service latency penalty. Paul et al. (U.S. 6,721,878)

discloses low-latency interrupt handling during memory access delay periods in microprocessors. Stevens (U.S. 6,338,111) discloses a method and apparatus for reducing I/O interrupts. Kailash et al. (U.S. 6,185,639) discloses a system and method to reduce a computer system's interrupt processing overhead. Binford et al. (U.S. 5,671,365) discloses an I/O system for reducing main processor overhead in initiating I/O requests and servicing I/O completion events. Bashford (U.S. 6,629,179) discloses a message signaled interrupt generating device and method. Constantinos Dovrolis, Brad Thayer, and Parameswaran Ramanathan (ACM SIGOPS Operating Systems Review, Volume 35, Issue 4) disclose a method for hybrid interrupt-polling for the network interface.

10. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Faisal Zaman whose telephone number is 571-272-6495. The examiner can normally be reached on Monday thru Friday, 9 am – 5:30 pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Rehana Perveen can be reached on 571-272-3676. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

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